— APPENDIX B —

MEMORY MAP

Usage

The information in this appendix provides a useful reference to the memory locations of the Atari computer series. While most documented locations have stayed backwardly compatible, some have changed in meaning. Software programmers directly accessing these locations should carefully consider the possibility that a location may move or not even exist in a newer version of the OS. For this reason many OS functions exist to manipulate system variables, vectors, interrupts, and devices. These should always be used, if possible, as an alternative to directly accessing hardware registers, vectors, interrupts, and variables.

WARNING!

In addition to those considerations mentioned above, directly accessing hardware registers can cause damage to hardware if not done correctly. In particular, improper use of the Falcon030 video registers could damage an attached monitor. Likewise, use of the floppy and hard drive registers can cause data loss and drive damage. For these reasons, it is strongly recommended that you avoid using hardware registers when possible, and when otherwise unavoidable, they should be used with extreme care.

Memory Map Conventions

For each Atari computer that a specific hardware location is valid for, the appropriate box will be shaded. Following is a key to several abbreviations and concepts used in this guide:

BYTE	Occupies one byte (8 bits).
WORD	Occupies one **WORD** (16 bits).
LONG	Occupies one longword (32 bits).
OW	Occupies the odd **WORD** of a **LONG**.
EW	Occupies the even **WORD** of a **LONG**.
OB	Occupies the odd **BYTE** of a **WORD**.
EB	Occupies the even **BYTE** of the **WORD**.
ROM	Location is Read-Only Memory
RAM	Location is Read-Write Memory
I/O	Location is hardware-mapped
VME	Location addresses VME address space
N/A	Not applicable
RO	Read-only location
WO	Write-only location
RW	Read-write location
RSVD	Reserved
Unassigned	Either not assigned or undocumented (hardware developers should always consult Atari before mapping a third-party device to a hardware location).

B.4 – Memory Map

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
System Boot Variables									
0x00000000	**LONG**							ROM	Reset: Supervisor Stack Pointer
0x00000004	**LONG**							ROM	Reset: Program Counter
68x00 Exception Vectors									
0x00000008	**LONG**							RAM	Bus Error Vector
0x0000000C	**LONG**							RAM	Address Error Vector
0x00000010	**LONG**							RAM	Illegal Instruction Error Vector
0x00000014	**LONG**							RAM	Divide by 0 Error Vector
0x00000018	**LONG**							RAM	CHK Instruction Exception Vector
0x0000001C	**LONG**							RAM	TRAPV, FTRAPcc, TRAPcc, cpTRAPcc Instruction Exception Vector
0x00000020	**LONG**							RAM	Privilege Violation Exception Vector
0x00000024	**LONG**							RAM	Trace Exception Vector
0x00000028	**LONG**							RAM	Line-A Exception Vector
0x0000002C	**LONG**							RAM	Line-F Exception Vector
0x00000030	**LONG**							RAM	Reserved by Motorola
0x00000034	**LONG**							RAM	Coprocessor Protocol Violation Vector
0x00000038	**LONG**							RAM	Format Error Vector
0x0000003C	**LONG**							RAM	Uninitialized Interrupt Vector
0x00000040 – 0x0000005C	**LONG**							RAM	Reserved by Motorola
0x00000060	**LONG**							RAM	Spurious Interrupt Vector (taken when an interrupt occurs during Bus Error handling)
Auto-Vector Interrupts									
0x00000064	**LONG**							RAM	Level 1 Auto-Vector Interrupt (used if Hblank is enabled)
0x00000068	**LONG**							RAM	Level 2 Auto-Vector Interrupt (Hblank)
0x0000006C	**LONG**							RAM	Level 3 Auto-Vector Interrupt (Normal processor interrupt level)
0x00000070	**LONG**							RAM	Level 4 Auto-Vector Interrupt (Vblank)
0x00000074	**LONG**							RAM	Level 5 Auto-Vector Interrupt (currently unused)
0x00000078	**LONG**							RAM	Level 6 Auto-Vector Interrupt (MFP Interrupts)
0x0000007C	**LONG**							RAM	Level 7 Auto-Vector Interrupt (Non-maskable)
TRAP Exception Vectors									
0x00000080	**LONG**							RAM	TRAP #0 Handler (Currently Unused)
0x00000084	**LONG**							RAM	TRAP #1 Handler (**GEMDOS**)
0x00000088	**LONG**							RAM	TRAP #2 Handler (**AES** and **VDI**)

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x0000008C	**LONG**							RAM	TRAP #3 Handler (Currently Unused)
0x00000090	**LONG**							RAM	TRAP #4 Handler (Currently Unused)
0x00000094	**LONG**							RAM	TRAP #5 Handler (Currently Unused)
0x00000098	**LONG**							RAM	TRAP #6 Handler (Currently Unused)
0x0000009C	**LONG**							RAM	TRAP #7 Handler (Currently Unused)
0x000000A0	**LONG**							RAM	TRAP #8 Handler (Currently Unused)
0x000000A4	**LONG**							RAM	TRAP #9 Handler (Currently Unused)
0x000000A8	**LONG**							RAM	TRAP #10 Handler (Currently Unused)
0x000000AC	**LONG**							RAM	TRAP #11 Handler (Currently Unused)
0x000000B0	**LONG**							RAM	TRAP #12 Handler (Currently Unused)
0x000000B4	**LONG**							RAM	TRAP #13 Handler (**BIOS**)
0x000000B8	**LONG**							RAM	TRAP #14 Handler (**XBIOS**)
0x000000BC	**LONG**							RAM	TRAP #15 Handler (Currently Unused)
68881 Co-processor Exception Vectors									
0x000000C0	**LONG**							RAM	FPCP Branch or Set on Unordered Condition Vector
0x000000C4	**LONG**							RAM	FPCP Inexact Result Vector
0x000000C8	**LONG**							RAM	FPCP Floating-Point Divide by Zero Vector
0x000000CC	**LONG**							RAM	FPCP Underflow Vector
0x000000D0	**LONG**							RAM	FPCP Operand Error Vector
0x000000D4	**LONG**							RAM	FPCP Overflow Vector
0x000000D8	**LONG**							RAM	FPCP Signaling NAN Vector
0x000000DC	**LONG**							RAM	Unassigned
68851 MMU Exception Vectors									
0x000000E0	**LONG**							RAM	MMU Configuration Error Vector
0x000000E4	**LONG**							RAM	MMU Illegal Operation Vector
0x000000E8	**LONG**							RAM	MMU Access Violation Vector
0x000000EC – 0x000000FC	**LONG**							RAM	Reserved by Motorola
Multi-Function Peripheral Port Vectors									
0x00000100	**LONG**							RAM	MFP #0: Parallel-Port Interrupt Vector
0x00000104	**LONG**							RAM	MFP #1: RS-232 Carrier Detect Vector (On a Falcon030, this MFP interrupt is connected to the parallel port 'Acknowledge' signal, not the RS-232 port.)
0x00000108	**LONG**							RAM	MFP #2: RS-232 Clear to Send Vector
0x0000010C	**LONG**							RAM	MFP #3: BLiTTER Operation Complete (when hardware BLiTTER is present)

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00000110	**LONG**							RAM	Timer D: RS-232 Baud Rate Generator
0x00000114	**LONG**							RAM	Timer C: 200 Hz System Clock
0x00000118	**LONG**							RAM	MFP #4: Keyboard/MIDI (6850 processor)
0x0000011C	**LONG**							RAM	MFP #5: Floppy/Hard Disk Controller
0x00000120	**LONG**							RAM	Timer B: Horizontal Blank Counter
0x00000124	**LONG**							RAM	RS-232 Transmit Error Interrupt
0x00000128	**LONG**							RAM	RS-232 Transmit Buffer Error Interrupt
0x0000012C	**LONG**							RAM	RS-232 Receive Error Interrupt
0x00000130	**LONG**							RAM	RS-232 Receive Buffer Full Interrupt
0x00000134	**LONG**							RAM	Timer A: DMA Sound Complete
0x00000138	**LONG**							RAM	MFP #6: RS-232 Ring Indicator (On a Falcon030, this is the only Serial port vector that remains part of the MFP. All other Serial port functions have been transferred to the SCC.)
0x0000013C	**LONG**							RAM	MFP #7: Monochrome Monitor Detect
Multi-Function Peripheral Port Vectors (TT)									
0x00000140	**LONG**							RAM	MFP #0: General Purpose I/O Pin
0x00000144	**LONG**							RAM	MFP #1: General Purpose I/O Pin
0x00000148	**LONG**							RAM	MFP #2: SCC DMAC Interrupt
0x0000014C	**LONG**							RAM	MFP #3: RS-232 Ring Indicator
0x00000150	**LONG**							RAM	Timer D: RS-232 Baud Rate Generator
0x00000154	**LONG**							RAM	Timer C: SCC TRxCB
0x00000158	**LONG**							RAM	MFP #4: Reserved
0x0000015C	**LONG**							RAM	MFP #5: SCSI DMAC Interrupt
0x00000160	**LONG**							RAM	Timer B: Unassigned
0x00000164	**LONG**							RAM	RS-232 Transmit Error Interrupt
0x00000168	**LONG**							RAM	RS-232 Transmit Buffer Error Interrupt
0x0000016C	**LONG**							RAM	RS-232 Receive Error Interrupt
0x00000170	**LONG**							RAM	RS-232 Receive Buffer Error Interrupt
0x00000174	**LONG**							RAM	Timer A: Reserved
0x00000178	**LONG**							RAM	MFP #6: RTC IRQ
0x0000017C	**LONG**							RAM	MFP #7: SCSI Controller IRQ
Zilog 85C30 (SCC) Interrupt Vectors									
0x00000180	**LONG**							RAM	SCC Port B Transmit Buffer Empty Vector
0x00000184	**LONG**							RAM	Unused
0x00000188	**LONG**							RAM	SCC Port B External Status Change Vector
0x0000018C	**LONG**							RAM	Unused

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00000190	**LONG**							RAM	SCC Port B Receive Character Available Vector
0x00000194	**LONG**							RAM	Unused
0x00000198	**LONG**							RAM	SCC Port B Special Receive Condition Vector
0x0000019C	**LONG**							RAM	Unused
0x000001A0	**LONG**							RAM	SCC Port A Transmit Buffer Empty Vector
0x000001A4	**LONG**							RAM	Unused
0x000001A8	**LONG**							RAM	SCC Port A External Status Change Vector
0x000001AC	**LONG**							RAM	Unused
0x000001B0	**LONG**							RAM	SCC Port A Receive Character Available Vector
0x000001B4	**LONG**							RAM	Unused
0x000001B8	**LONG**							RAM	SCC Port A Special Receive Condition Vector
0x000001BC	**LONG**							RAM	Unused
0x000001C0 – 0x0000037F	**N/A**							RAM	Undefined
Processor State Save Area									
0x00000380	**LONG**							RAM	*proc_lives*: If, after a system failure, the operating system is able to save the processor state in the following variables, this value will be 0x12345678.
0x00000384	**LONG**							RAM	*proc_dregs*: The contents of registers D0 through D7 are stored here.
0x000003A4	**LONG**							RAM	*proc_aregs*: The contents of registers A0 through A7 are stored here.
0x000003C4	**LONG**							RAM	*proc_pc*: The first byte of this longword indicates the exception number that occurred.
0x000003C8	**LONG**							RAM	*proc_usp*: The user stack pointer (USP) is saved here.
0x000003CC– 0x000003EA	**WORD**							RAM	*proc_stk*: The top 16 **WORD**s of the supervisor stack are saved here.
0x000003EC – 0x000003FF	**N/A**							RAM	Unassigned
System Vectors									
0x00000400	**LONG**							RAM	*etv_timer*: System Timer Handoff Vector (see **GEMDOS**)
0x00000404	**LONG**							RAM	*etv_critic*: Critical Error Handoff Vector (see **GEMDOS**)
0x00000408	**LONG**							RAM	*etv_term*: Process Termination Handler (see **GEMDOS**)
0x0000040C – 0x0000041C	**LONG**							RAM	Reserved for future vectors.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
System Variables									
0x00000420	**LONG**							RAM	*memvalid*: If this variable is equal to $752019F3 and the value at *memval2* ($43A) is also correct, then the last coldstart was successful and *memcntlr* ($424) is valid. As of **TOS** 1.02 memval3 ($51A) must also be correct.
0x00000424	**WORD**							RAM	*memcntlr*: Bits 11–8 of this **WORD** contains the memory controller state.
0x00000426	**LONG**							RAM	*resvalid:* If this location contains the magic number $31415926 then the system will jump through *resvector* (below) on a system reset.
0x0000042A	**LONG**							RAM	*resvector*: If the magic number in *resvalid* is set properly, this vector will be jumped through on a system reset with the return address placed in A6.
0x0000042E	**LONG**							RAM	*phystop*: Physical top of ST compatible RAM.
0x00000432	**LONG**							RAM	*_membot*: This value points to the lowest memory location available for the system heap. This value is used to initialize **GEMDOS** free memory.
0x00000436	**LONG**							RAM	*_memtop*: This value points to the highest memory location available for the system heap. This value is used to initialize **GEMDOS** free memory.
0x0000043A	**LONG**							RAM	*memval2*: This value will equal $237698AA if coldstart was successful. See *memvalid* ($420).
0x0000043E	**WORD**							RAM	*flock*: This variable should be set to non-zero prior to accessing the DMA registers to prevent the system or other processes from attempting DMA concurrently.
0x00000440	**WORD**							RAM	*seekrate*: This variable sets the floppy drive seek rate for both floppy drives as follows: **Value** — **Seek Rate** 0 — 6 ms 1 — 12 ms 2 — 2 ms 3 — 3 ms (default)
0x00000442	**WORD**							RAM	*_timr_ms*: This value indicates the time between system timer ticks in milliseconds. Current machines have the value of 20 (0x14) equating to 50 timer updates per second. This value is returned by the **BIOS** function **Tickcal()** and is placed on the stack prior to jumping through the timer handoff vector ($400).

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00000444	**WORD**							RAM	*_fverify*: When non-zero, all floppy writes are verified, otherwise, no verification is done.
0x00000446	**WORD**							RAM	*_bootdev*: This value represents the device from which the system was booted (0 = A:, 1 = B:, etc.)
0x00000448	**WORD**							RAM	*palmode*: A value of 0 indicates that NTSC video is being used, otherwise, PAL is being is used.
0x0000044A	**WORD**							RAM	*defshftmd*: This value indicates the default video shifter mode.
0x0000044C	**WORD**							RAM	*sshiftmd*: This value is a copy of the hardware register at 0x00FF8260 which indicates the current ST shifter mode.
0x0000044E	**LONG**							RAM	*_v_bas_ad*: This indicates the starting address of the logical screen. Prior to **TOS** 1.06, this address needed to be aligned on a 256 byte boundary. As of **TOS** 1.06, it may be **WORD** aligned.
0x00000452	**WORD**							RAM	*vblsem*: A value of 0 here disables all vertical blank processing while a value of 1 enables it.
0x00000454	**WORD**							RAM	*nvbls*: This value indicates the number of slots in the deferred vertical blank handler list. If all table slots are full and your application needs to install a handler, it may allocate a new, larger list, update this value and the pointer below.
0x00000456	**LONG**							RAM	*_vblqueue*: This is a pointer to a list of pointers to the deferred vertical blank handlers. Each pointer in the list pointed to by this variable which contains a value other than 0 is 'JSR'ed' through at each vertical blank. This occurs 50 times per second on PAL color monitors, 60 times per second on NTSC color monitors and 70 times per second on all monochrome monitors.
0x0000045A	**LONG**							RAM	*colorptr*: If this value is non-zero then at the next vertical blank, the 16 color registers pointed to by this value will be loaded into the hardware registers.
0x0000045E	**LONG**							RAM	*screenpt*: If this value is non-zero then at the next vertical blank, the value stored here will be loaded into the hardware register which points to the base of the physical screen.
0x00000462	**LONG**							RAM	*_vbclock*: This value indicates the number of vertical blanks that have been processed since the last reset.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00000466	**LONG**							RAM	*_frlock*: This value indicates the number of vertical blanks regardless of whether they were processed or not (blocked by *vblsem*).
0x0000046A	**LONG**							RAM	*hdv_init*: This value points the hard disk initialization routine or is 0 to indicate that no hard disk is installed.
0x0000046E	**LONG**							RAM	*swv_vec*: The vector pointed to by this routine is called when the system detects a change in monitors (normally this points to the reset handler).
0x00000472	**LONG**							RAM	*hdv_bpb*: This vector is used when **Getbpb()** is called. A value of 0 indicates that no hard disk is attached. Applications installing themselves here should expect parameters to be located on the stack as they would be for the actual function call beginning at 4(sp). If the installed process services the call it should RTS, otherwise, leaving the stack intact, should JMP through the old vector value.
0x00000476	**LONG**							RAM	*hdv_rw*: This vector is used when **Rwabs()** is called. A value of 0 here indicates that no hard disk is attached. Applications installing themselves here should expect parameters to be located on the stack as they would be for the actual function call beginning at 4(sp). If the installed process services the call it should RTS, otherwise, leaving the stack intact, should JMP through the old vector value.
0x0000047A	**LONG**							RAM	*hdv_boot*: This vector is JSR'ed through to boot from the hard disk. A value of 0 here indicates that no hard disk is attached. If the installed process services the call it should RTS, otherwise, leaving the stack intact, should JMP through the old vector value.
0x0000047E	**LONG**							RAM	*hdv_mediach*: This vector is used when **Mediach()** is called. A value of 0 here indicates that no hard disk is attached. Applications installing themselves here should expect parameters to be located on the stack as they would be for the actual function call beginning at 4(sp). If the installed process services the call it should RTS, otherwise, leaving the stack intact, should JMP through the old vector value.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00000482	**WORD**							RAM	*_cmdload*: During boot if this location contains a non-zero value, the system will attempt to load "COMMAND.PRG" from the boot device rather than initializing the **GEM** Desktop.
0x00000484	**BYTE**							RAM	*conterm*: This location contains a bit array which determine several system attributes as follows: **Bit** — **Meaning if Set** 0 — Enable key-click 1 — Enable key repeat 2 — Enable system bell 3 — Cause **Bconin**() to return shift status
0x00000485	**BYTE**							RAM	Reserved
0x00000486	**LONG**							RAM	*trp14ret*: This value is used by Trap #14 OS code to store the return address.
0x0000048A	**LONG**							RAM	*criticret*: This value is used by *etv_critic* handling code to store the return address.
0x0000048E – 0x0000049D	**BYTE**							RAM	*themd*: This is the **MD** (Memory Descriptor structure) initialized by the **BIOS** at boot and returned by **Getmpb()**.
0x0000049E	**LONG**							RAM	*_md*: This is a pointer to additional **MD** structures.
0x000004A2	**LONG**							RAM	*savptr*: This is a pointer to the buffer which the **BIOS** uses to save internal registers.
0x000004A6	**WORD**							RAM	*_nflops*: This value indicates the number of floppy drives currently connected to the system.
0x000004A8	**LONG**							RAM	*con_state*: This is a vector to internal console output routines which is set to various VT-52 ESC functions.
0x000004AC	**WORD**							RAM	*save_row*: This value contains the row number of the cursor temporarily when using the ESC-Y VT-52 sequence.
0x000004AE	**LONG**							RAM	*sav_contxt*: This points to a temporary buffer where the processor context is saved.
0x000004B2 – 0x000004B6	**LONG**							RAM	*_bufl*: The first longword here points to a **BCB** (Buffer Control Block) used to store data sectors. The second longword points to a **BCB** which is used to store FAT and directory sectors.
0x000004BA	**LONG**							RAM	*_hz_200*: This value is an ongoing counter for the internal 200Hz clock. It is used as a seed value for the **Random()** function.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x000004BE	**LONG**							RAM	*the_env*: This longword is the default environment string (four zeros).
0x000004C2	**LONG**							RAM	*_drvbits*: Each of 32 bits in this longword represents a drive connected to the system. Bit #0 is A, Bit #1 is B and so on. If at least one floppy is connected to the system, both floppy bits will always be set because of virtual swapping.
0x000004C6	**LONG**							RAM	*_dskbufp*: This variable points to a 1K disk operation buffer and is also used by some graphics functions.
0x000004CA	**LONG**							RAM	*_autopath*: This variable points to the **GEMDOS** path specification of the directory to load '\AUTO' folder programs from (may be **NULL** to indicate default).
0x000004CE – 0x000004EA	**LONG**							RAM	*_vbl_list*: This area is used by the system for the initial deferred vertical blank list.
0x000004EE	**WORD**							RAM	*_prt_cnt*: This value is used by the ALT-HELP screen dump code and is initialized to 0xFFFF. Each time ALT-HELP is pressed, this value is incremented. Custom screen dump code should check this value on entry and if 0 begin a screen dump, otherwise, abort the dump, reset the value to 0xFFFF and return.
0x000004F0	**WORD**							RAM	*_prtabt*: Flag is set to abort printing because of a timeout.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning

0x000004F2	**LONG**							RAM	*_sysbase*: This value points to the beginning of the **TOS** operating system. The beginning of the OS contains a structure as follows:
									
									`typedef struct _osheader`
									`{`
									`/* BRA to Reset Code */`
									`UWORD os_entry;`
									`/* TOS Version */`
									`UWORD os_version;`
									`/* Reset Code */`
									`VOID *reseth;`
									`/* Pointer to OSBASE */`
									`struct _osheader *os_beg;`
									`/* Pointer to OS end*/`
									`VOID *os_end;`
									`/* Reserved */`
									`LONG os_rsv1;`
									`/* Memory Usage PB */`
									`GEM_MUPB *os_magic;`
									`/* OS Date $YYYYMMDD */`
									`LONG os_date;`
									`/* OS Conf. Bits */`
									`UWORD os_conf;`
									`/* DOS OS Date */`
									`UWORD os_dosdate;`
									
									`/* As of TOS 1.2 */`
									
									`/* Base of OS Pool */`
									`char **p_root;`
									`/* Key. Shift State */`
									`char **pkbshift;`
									`/* Current process */`
									`BASEPAGE **p_run;`
									`/* Reserved */`
									`char *p_rsv2;`
									`} OSHEADER;`

0x000004F6	**LONG**							RAM	*_shell_p*: Normally not utilized, this vector allows a shell process to be installed which expects to be called with a pointer to a CLI-type command to be at 4(sp). If a command handler does not exist, this value will be **NULL**.
0x000004FA	**LONG**							RAM	*end_os*: This value points to the end of RAM utilized by **TOS** (copied into *membot*).

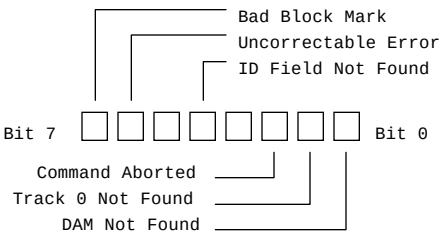
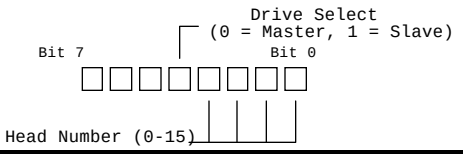
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x000004FE	**LONG**							RAM	*exec_os*: This vector is jumped through when operating system initialization is complete (normally points to the Desktop/**AES** startup code).
0x00000502	**LONG**							RAM	*scr_dump*: The routine pointed to by this value is called each time the user pressed ALT-HELP.
0x00000506	**LONG**							RAM	*prv_lsto*: This vector is called to check the status of the 'PRN:' output device by the **Prtblk()** routine.
0x0000050A	**LONG**							RAM	*prv_lst*: This vector is called to output a byte to the 'PRN:' device by the **Prtblk()** routine..
0x0000050E	**LONG**							RAM	*prv_auxo*: This vector is called to check the status of the 'AUX:' output device by the **Prtblk()** routine.
0x00000512	**LONG**							RAM	*prv_aux*: This vector is called to output a byte to the 'AUX:' device by the **Prtblk()** routine.

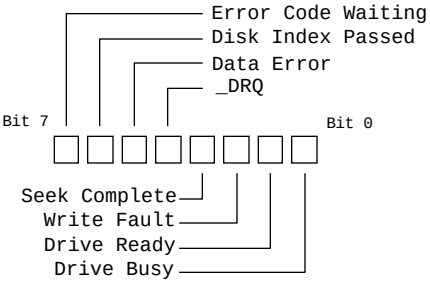
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning

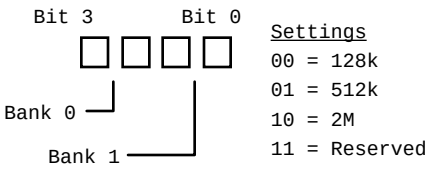
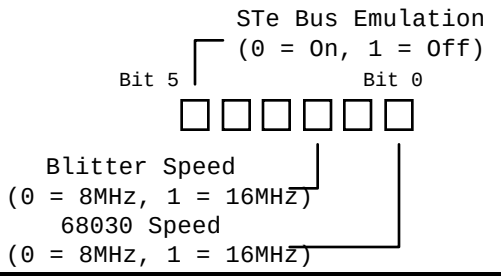
0x00000516	**LONG**							RAM	*pun_ptr*: This points to a structure used by AHDI as follows:
									
									`/* # supported drives */`
									
									`#define MAXUNITS 16`
									
									`typedef struct`
									`{`
									`  /* Maximum # of drives`
									`   * supported by system,`
									`   * including floppies.`
									`   */`
									`  WORD puns;`
									`  /* Bit 0-2 indicates`
									`   * the physical ACSI unit`
									`   * it resides on.`
									`   * Bit 7 = 0 indicates`
									`   * that the drive exists`
									`   */`
									`  BYTE pun[MAXUNITS];`
									`  /* Indicates offset in`
									`   * physical sectors (512`
									`   * bytes) to the start of`
									`   * partition.`
									`   */`
									`  LONG prt_start[MAXUNITS];`
									
									`  /* The following are`
									`   * only present as of`
									`   * AHDI 3.0. */`
									
									`  /* Cookie is $41484449 */`
									`  LONG P_cookie;`
									`  /* Points to P_cookie */`
									`  LONG *P_cookptr;`
									`  /* Version of AHDI */`
									`  UWORD P_version;`
									`  /* Size of the largest`
									`   * logical sector. */`
									`  UWORD P_max_sector;`
									`  /* Reserved */`
									`  LONG reserved[MAXUNITS];`
									`} PUN_INFO;`

0x0000051A	**LONG**							RAM	*memval3*: Will equal $5555AAAA if coldstart was successful. See *memvalid* ($420).

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x0000051E – 0x0000053A	**LONG**							RAM	*xconstat*: This location contains eight pointers to the **BIOS Bconstat()** functions for eight **BIOS** devices.
0x0000053E – 0x0000055A	**LONG**							RAM	*xconin*: This location contains eight pointers to the **BIOS Bconin()** functions for eight **BIOS** devices.
0x0000055E – 0x0000056A	**LONG**							RAM	*xcostat*: This location contains eight pointers to the **BIOS Bcostat()** functions for eight **BIOS** devices.
0x0000057E – 0x0000059A	**LONG**							RAM	*xconout*: This location contains eight pointers to the **BIOS Bconout()** functions for eight **BIOS** devices.
0x0000059E	**WORD**							RAM	*_longframe*: If this value is 0 then the processor uses short stack frames, otherwise it uses long stack frames. This value is of interest to applications which intercept TRAP handlers. When using short stack frames, the first parameter will be found at 6(sp), otherwise at 8(sp).
0x000005A0	**LONG**							RAM	*_p_cookies*: This is a pointer to the system Cookie Jar.
0x000005A4	**LONG**							RAM	*ramtop*: If *ramvalid* is correct, this is a pointer to the end of alternative RAM.
0x000005A8	**LONG**							RAM	*ramvalid*: This value should be $1357BD13 to indicate that *ramtop* is correct.
0x000005AC	**LONG**							RAM	*bell_hook*: This vector is jumped through to sound the system bell.
0x000005B0	**LONG**							RAM	*kcl_hook*: This vector is jumped through to sound system key clicks. The scancode of the current character is placed in the low byte of D0.
System RAM / Expansion									
0x000005B4 – 0x009FFFFF	**BYTE**							RAM/ ROM	This area contains whatever remaining ST compatible RAM is available. Additional space at this location is utilized by the operating system. Memory locations below 0x00E00000 on a machine other than the Mega STe or below 0x00A00000 on a Mega STe that are not part of this RAM may be utilized by hardware developers.
0x00A00000 – 0x00DEFFFF	**BYTE**							VME/ RAM	On a Mega STe, this area is mapped to VME A24:D16 address space, otherwise it may be mapped to additional ST compatible RAM or I/O space. Falcon030 computers use this address space for RAM.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00DF0000 – 0x00DFFFFF	**BYTE**							VME/ RAM	On a Mega STe, this area is mapped to VME A16:D16 address space, otherwise it may be mapped to additional ST compatible RAM or I/O space. Falcon030 computers use this address space for RAM.
0x00E00000 – 0x00EFFFFF	**BYTE**							ROM	Operating system ROM's as of **TOS** 1.06.
IDE Controller									
0x00F00000	**OW**							I/O	Data Register
0x00F00004	**OB**							I/O	Error Register as follows: 
0x00F00006	**N/A**								Unused
0x00F00008	**OB**							I/O	Sector Count Register
0x00F0000A	**N/A**							I/O	Unused
0x00F0000C	**OB**							I/O	Sector Number Register
0x00F0000E	**N/A**							I/O	Unused
0x00F00010	**OB**							I/O	Cylinder Low Register (this register is written with the low eight bits of the ten bit cylinder number).
0x00F00012	**N/A**							I/O	Unused
0x00F00014	**OB**							I/O	Cylinder High Register (this register is written with the high two bits of the ten bit cylinder number).
0x00F00016	**N/A**							I/O	Unused
0x00F00018	**OB**							I/O	Drive Head Register as follows: 

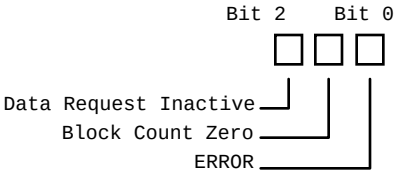
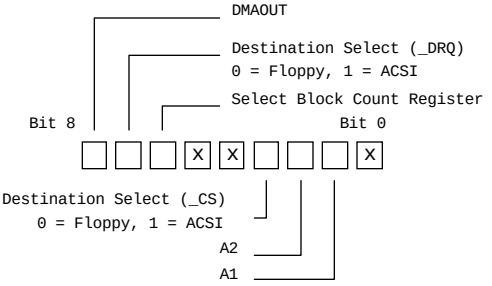
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00F0001A – 0x00F0001D	**N/A**							I/O	Unused
0x00F0001E	**OB**							I/O	Status Register (on read) as follows:  Command Register (on write). The IDE registers must be completely setup prior to writing the command byte here.
0x00F00020 – 0x00F00036	**N/A**							I/O	Unused
0x00F00038	**OB**							I/O	Alternate Status Register (on read) Alternate Command Register (on write)
0x00F00040 – 0x00F9FFFF	**N/A**							N/A	Unassigned
ROM/Reserved Hardware Space									
0x00FA0000 – 0x00FBFFFF	**BYTE**							ROM	Cartridge ROM
0x00FC0000 – 0x00FEFFFF	**BYTE**							ROM	On pre **TOS** 2.00 machines, this location marked the beginning of the operating system ROM's.
0x00FF0000 – 0x00FF7FFF	**N/A**							N/A	Unassigned

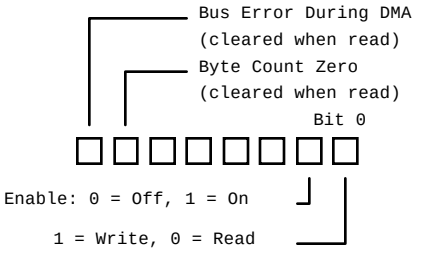
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
Memory Management Unit/Falcon Processor Control									
0x00FF8000	**OB**							I/O	Memory Controller Configuration as follows: 
0x00FF8002 – 0x00FF8004	**N/A**							I/O	Unassigned
0x00FF8006	**BYTE**							I/O	Connected Monitor Type as follows: **Value** **Monitor** 0 Atari Monochrome 1 Atari Color 2 VGA Color 3 Television
0x00FF8007	**BYTE**							I/O	Falcon Processor Control as follows: 
0x00FF8008 – 0x00FF81FF	**N/A**							I/O	Unassigned
Video Registers									
0x00FF8200	**OB**							I/O	Video Base Address High
0x00FF8202	**OB**							I/O	Video Base Address Mid
0x00FF8204	**OB**							I/O	Video Address Counter High (R/O)
0x00FF8206	**OB**							I/O	Video Address Counter Mid (R/O)
0x00FF8208	**OB**							I/O	Video Address Counter Low (R/O)

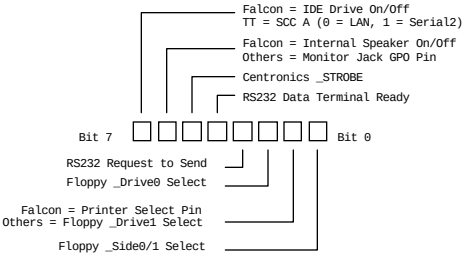
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF820A	**BYTE**							I/O	Video Shifter Sync Mode as follows: Bit 7 Bit 0 1= 60 Hz, 0 = 50 Hz 1 = External, 0 = Internal Sync
0x00FF820C	**OB**							I/O	Video Base Address Low
0x00FF820E	**OB**							I/O	Line Width Register (width of scanline in **WORD**s - 1). On a Falcon030, this is a **WORD** value.
0x00FF8210	**WORD**							I/O	Falcon030 Line Width Register (width of scanline in **WORD**s)
0x00FF8212 – 0x00FF823F	**N/A**							I/O	Unassigned
0x00FF8240	**WORD**							I/O	ST/e Compatible Palette Register #0: ST layout is as follows: XXXX XRRR XGGG XBBB STe layout is as follows: XXXX RRRR GGGG BBBB For compatibility, STe bit arrangement per nibble is 0-3-2-1. These registers are simulated for compatibility on newer model machines.
0x00FF8242	**WORD**							I/O	ST/e Compatible Palette Register #1
0x00FF8244	**WORD**							I/O	ST/e Compatible Palette Register #2
0x00FF8246	**WORD**							I/O	ST/e Compatible Palette Register #3
0x00FF8248	**WORD**							I/O	ST/e Compatible Palette Register #4
0x00FF824A	**WORD**							I/O	ST/e Compatible Palette Register #5
0x00FF824C	**WORD**							I/O	ST/e Compatible Palette Register #6
0x00FF824E	**WORD**							I/O	ST/e Compatible Palette Register #7
0x00FF8250	**WORD**							I/O	ST/e Compatible Palette Register #8
0x00FF8252	**WORD**							I/O	ST/e Compatible Palette Register #9
0x00FF8254	**WORD**							I/O	ST/e Compatible Palette Register #10
0x00FF8256	**WORD**							I/O	ST/e Compatible Palette Register #11
0x00FF8258	**WORD**							I/O	ST/e Compatible Palette Register #12
0x00FF825A	**WORD**							I/O	ST/e Compatible Palette Register #13

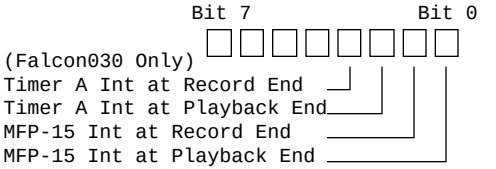
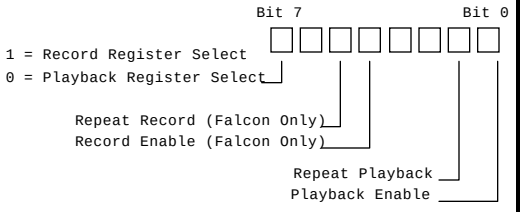
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF825C	**WORD**							I/O	ST/e Compatible Palette Register #14
0x00FF825E	**WORD**							I/O	ST/e Compatible Palette Register #15
0x00FF8260	**EB**							I/O	ST Video Shifter Mode as follows: Bit 7 ☐☐☐☐☐☐☐☐ Bit 0 00 = 320x200, 4 plane 01 = 640x200, 2 plane 10 = 640x400, 1 plane 11 = Reserved
0x00FF8262	**EB**							I/O	TT030 Video Shifter Mode as follows: Smear Mode Hyper Mono Mode Bit 15 ☐☐☐☐☐☐☐☐ Bit 8 000 = 320x200, 4 plane 001 = 640x200, 2 plane 010 = 640x400, 1 plane 100 = 640x480, 4 plane 110 = 1280x960, 1 plane 111 = 320x480, 8 plane Bit 7 ☐☐☐☐☐☐☐☐ Bit 0 ST Palette Bank
0x00FF8264	**OB**							I/O	Horizontal Scroll Register
0x00FF8266	**WORD**							I/O	SPSHIFT Control Register as follows: **Bit** — **Meaning When Set** 4 — Enable Bitplane Mode 5 — Use External VSYNC 6 — Use External HSYNC 8 — Enable Truecolor Mode 10 — Enable 2-Color Mode
0x00FF8268 – 0x00FF827D	**N/A**								Unassigned

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF827E	**EB**							I/O	STACY Display State as follows: Bit 7 Bit 0 1 = Backlight Off 1 = Display Off
0x00FF8280	**WORD**							I/O	Horizontal Hold Counter
0x00FF8282	**WORD**							I/O	Horizontal Hold Timer
0x00FF8284	**WORD**							I/O	Horizontal Border Begin
0x00FF8286	**WORD**							I/O	Horizontal Border End
0x00FF8288	**WORD**							I/O	Horizontal Display Begin
0x00FF828A	**WORD**							I/O	Horizontal Display End
0x00FF828C	**WORD**							I/O	HSS
0x00FF828E	**WORD**							I/O	HFS
0x00FF8290	**WORD**							I/O	HEE
0x00FF8292 – 0x00FF829F	**N/A**								Unassigned
0x00FF82A0	**WORD**							I/O	Vertical Frequency Counter
0x00FF82A2	**WORD**							I/O	Vertical Frequency Timer
0x00FF82A4	**WORD**							I/O	Vertical Border Begin
0x00FF82A6	**WORD**							I/O	Vertical Border End (in half lines)
0x00FF82A8	**WORD**							I/O	Vertical Display Begin
0x00FF82AA	**WORD**							I/O	Vertical Display End
0x00FF82AC	**WORD**							I/O	VSS
0x00FF82AE – 0x00FF82C1	**N/A**								Unassigned
0x00FF82C2	**WORD**							I/O	VCO - Video Control as follows: Bit 3 Bit 0 Quarter Pixel Width Halve Pixel Width Interlace Mode Line Doubling

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF82C4 – 0x00FF83FF	**N/A**							I/O	Unassigned
0x00FF8400 – 0x00FF85FE	**WORD**							I/O	TT030 Palette Registers #0 – #255: Each palette register is a longword which is arranged as follows: XXXX RRRR GGGG BBBB Unlike the ST registers, each nibble is properly formatted in the manner 3–2–1–0.
ACSI DMA and Floppy Disk Controller									
0x00FF8600 – 0x00FF8602	**WORD**							I/O	Reserved
0x00FF8604	**WORD**							I/O	DMA Sector Count (on write) DMA Data Register (on read)
0x00FF8606	**WORD**							I/O	DMA Status (on read) as follows:  DMA Mode Control (on write) as follows: 
0x00FF8608	**OB**							I/O	DMA Pointer High
0x00FF860A	**OB**							I/O	DMA Pointer Mid
0x00FF860C	**OB**							I/O	DMA Pointer Low
0x00FF860E – 0x00FF86FF	**N/A**							I/O	Unassigned

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
SCSI DMA Control									
0x00FF8700	**OB**							I/O	SCSI DMA Pointer Upper
0x00FF8702	**OB**							I/O	SCSI DMA Pointer Upper-Middle
0x00FF8704	**OB**							I/O	SCSI DMA Pointer Lower-Middle
0x00FF8706	**OB**							I/O	SCSI DMA Pointer Lower
0x00FF8708	**OB**							I/O	Byte Count Upper
0x00FF870A	**OB**							I/O	Byte Count Upper-Middle
0x00FF870C	**OB**							I/O	Byte Count Lower-Middle
0x00FF870E	**OB**							I/O	Byte Count Lower
0x00FF8710	**WORD**							I/O	SCSI DMA Data Residue Register High
0x00FF8712	**WORD**							I/O	SCSI DMA Data Residue Register Low
0x00FF8714	**OB**							I/O	SCSI DMA Control Register as follows: 
0x00FF8716 – 0x00FF877F	**N/A**							I/O	Unassigned
SCSI Controller Registers									
0x00FF8780	**OB**							I/O	SCSI Controller Data Register
0x00FF8782	**OB**							I/O	SCSI Controller Initiator Command Register
0x00FF8784	**OB**							I/O	SCSI Controller Mode Register
0x00FF8786	**OB**							I/O	SCSI Controller Target Command Register
0x00FF8788	**OB**							I/O	SCSI Controller ID Select/Control Register
0x00FF878A	**OB**							I/O	SCSI Controller DMA Start/DMA Status
0x00FF878C	**OB**							I/O	SCSI Controller DMA Target Receive/Input Data
0x00FF878E	**OB**							I/O	SCSI Controller DMA Initiator Receive/Reset
0x00FF8790 – 0x00FF879F	**N/A**							I/O	Unassigned

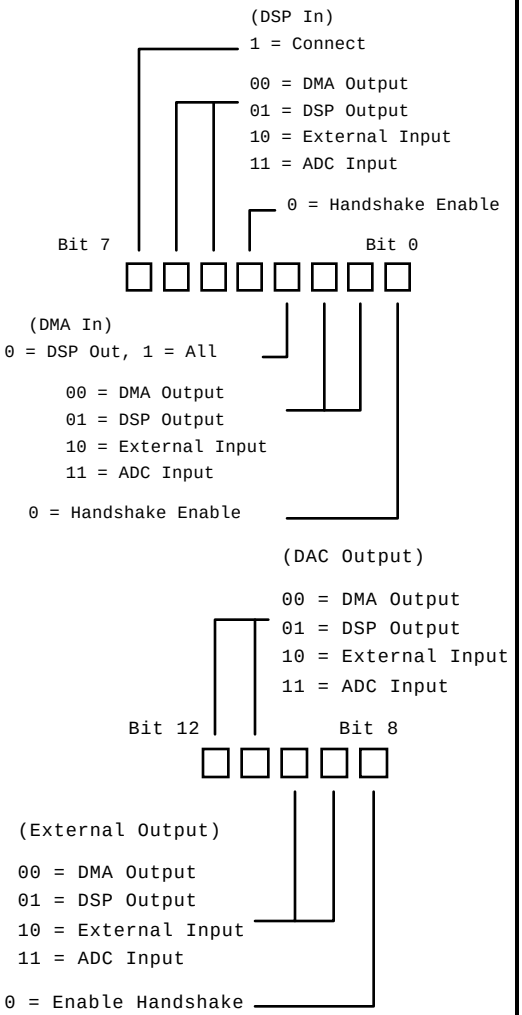
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
Programmable Sound Generator (YM-2149)									
0x00FF8800	**EB**							I/O	PSG Read (Read only on I/O port B) / PSG Register Select (WO). Reading this location yields data from the parallel interface. Writing to bits 0–3 of this location selects a PSG register to address as follows: **Value** **Register** 0000 Channel A Fine Tune 0001 Channel A Coarse Tune 0010 Channel B Fine Tune 0011 Channel B Coarse Tune 0100 Channel C Fine Tune 0101 Channel C Coarse Tune 0110 Noise Generator Control 0111 Mixer Control – I/O Enable 1000 Channel A Amplitude 1001 Channel B Amplitude 1010 Channel C Amplitude 1011 Envelope Period Fine Tune 1100 Envelope Period Coarse Tune 1110 I/O Port A Select (Write only) 1111 I/O Port B Select
0x00FF8802	**EB**							I/O	When I/O Port A is selected, this location contains the PSG Write Data (WO) register as follows:  When I/O Port B is selected, this locations accesses the Parallel Port Data Register (WO).
0x00FF8804 – 0x00FF88FF	**N/A**							I/O	Unassigned

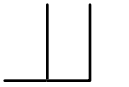
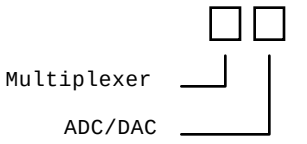
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
DMA Sound System									
0x00FF8900	**BYTE**							I/O	Sound DMA Control as follows: 
0x00FF8901	**BYTE**							I/O	Additional sound DMA control as follows: 
0x00FF8902	**OB**							I/O	Frame Base Address High
0x00FF8904	**OB**							I/O	Frame Base Address Mid
0x00FF8906	**OB**							I/O	Frame Base Address Low
0x00FF8908	**OB**							I/O	Frame Address Counter High
0x00FF890A	**OB**							I/O	Frame Address Counter Mid
0x00FF890C	**OB**							I/O	Frame Address Counter Low
0x00FF890E	**OB**							I/O	Frame End Address High
0x00FF8910	**OB**							I/O	Frame End Address Mid
0x00FF8912	**OB**							I/O	Frame End Address Low
0x00FF8914 – 0x00FF8919	**N/A**							I/O	Unassigned

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF8920	**BYTE**							I/O	Sound mode control as follows: 00 = Monitor Track 0 01 = Monitor Track 1 10 = Monitor Track 2 11 = Monitor Track 3 Bit 7 … Bit 0 00 = Play 1 Track 01 = Play 2 Tracks 10 = Play 3 Tracks 11 = Play 4 Tracks
0x00FF8921	**BYTE**							I/O	Additional sound mode control as follows: 00 = 8-bit Stereo 01 = 16-bit Stereo (Falcon) 10 = 8-bit Mono Bit 7 … Bit 0 00 = 6258 Hz 01 = 12517 Hz 10 = 25033 Hz 11 = 50066 Hz
MICROWIRE									
0x00FF8922	**WORD**							I/O	MICROWIRE Data Register
0x00FF8924	**WORD**							I/O	MICROWIRE Mask Register
0x00FF8926 – 0x00FF8929	**N/A**							I/O	Unassigned

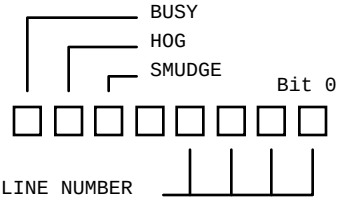
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
Falcon030 DSP/DMA Controller									
0x00FF8930	**WORD**							I/O	DMA Crossbar Output Select Controller as follows: (DSP Out) 1 = Connect 00 = 25.175 MHz Clock 01 = External Clock 10 = 32 MHz Clock 0 = Handshake Enable Bit 7 … Bit 0 (DMA Out) 0 = DMA In, 1 = All 00 = 25.175MHz Clock 01 = External Clock 10 = 32 MHz Clock 0 = Handshake Enable (ADC Input) 0 = Internal Sync 1 = External Sync Bit 12 … Bit 8 (External Input) 00 = 25.175 MHz Clock 01 = External Clock 10 = 32 MHz Clock 0 = Enable Handshake

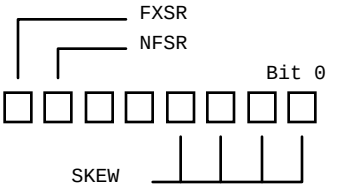
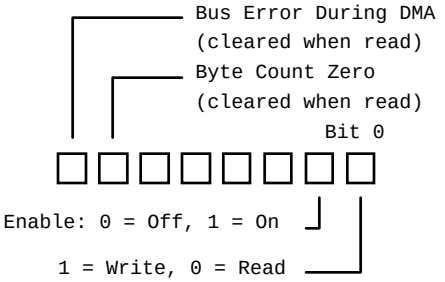
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF8932	**WORD**							I/O	DMA Crossbar Input Select Controller as follows:



Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF8934	**BYTE**							I/O	Frequency Divider External Sync (0 = STe/TT030 Compatible Prescaler, 1-15 = Divide by 256 and then the value given)
0x00FF8935	**BYTE**							I/O	Frequency Divider Internal Sync as follows: **Value** – **Meaning** 0 – STe Compatible Mode 1 – 49170 Hz 2 – 32780 Hz 3 – 24585 Hz 4 – 19668 Hz 5 – 16390 Hz 6 – 14049 Hz 7 – 12292 Hz 8 – 10927 Hz 9 – 9834 Hz 10 – 8940 Hz 11 – 8195 Hz 12 – 7565 Hz 13 – 7024 Hz 14 – 6556 Hz 15 – 6146 Hz
0x00FF8936	**BYTE**							I/O	Record Tracks Select as follows: Bit 1/0  00 = Record 1 Track 01 = Record 2 Tracks 10 = Record 3 Tracks 11 = Record 4 Tracks
0x00FF8937	**BYTE**							I/O	CODEC Input Source as follows: Bit 1/0  Multiplexer ADC/DAC

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF8938	**BYTE**							I/O	CODEC ADC Input as follows: Bit 1/0 0 = Left Channel Mic 1 = Left Channel PSG 0 = Right Channel Mic 1 = Right Channel PSG
0x00FF8939	**BYTE**							I/O	Gain settings (0–15 per channel) as follows: Bit 7 … Bit 0 L L L L R R R R
0x00FF893A	**BYTE**							I/O	Attenuation settings (0–15 per channel) as follows: Bit 7 … Bit 0 L L L L R R R R
0x00FF8940	**OB**							I/O	GPIO Data direction as follows: Bit 2 Bit 0 0 = Read 1 = Write
0x00FF8942	**OB**							I/O	GPIO Data (low three bits). Read or write by setting direction bits above.
0x00FF8944 – 0x00FF895F	**N/A**							I/O	Unassigned
Real Time Clock (146818A)									
0x00FF8960	**OB**							I/O	Real Time Clock Address Register
0x00FF8962	**OB**							I/O	Real Time Clock Data Register
0x00FF8964 – 0x00FF89FF	**N/A**							I/O	Unassigned

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
BLiTTER Bit-Block Transfer Processor									
0x00FF8A00 – 0x00FF8A1E	**WORD**							I/O	BLiTTER Halftone RAM
0x00FF8A20	**WORD**							I/O	BLiTTER Source X Increment
0x00FF8A22	**WORD**							I/O	BLiTTER Source Y Increment
0x00FF8A24	**WORD**							I/O	BLiTTER Source Address (bits 7–0 are bits 23–16 of address)
0x00FF8A26	**WORD**							I/O	BLiTTER Source Address (bits 15–1 are bits 15–1 of address, bit 0 must be 0)
0x00FF8A28	**WORD**							I/O	BLiTTER Endmask 1
0x00FF8A2A	**WORD**							I/O	BLiTTER Endmask 2
0x00FF8A2C	**WORD**							I/O	BLiTTER Endmask 3
0x00FF8A2E	**WORD**							I/O	BLiTTER Destination X Increment
0x00FF8A30	**WORD**							I/O	BLiTTER Destination Y Increment
0x00FF8A32	**WORD**							I/O	BLiTTER Destination (bits 7–0 are bits 23–16 of address)
0x00FF8A34	**WORD**							I/O	BLiTTER Destination (bits 15–1 are bits 15–1 of address, bit 0 must be 0)
0x00FF8A36	**WORD**							I/O	BLiTTER X Count
0x00FF8A38	**WORD**							I/O	BLiTTER Y Count
0x00FF8A3A	**BYTE**							I/O	BLiTTER HOP
0x00FF8A3B	**BYTE**							I/O	BLiTTER OP
0x00FF8A3C	**BYTE**							I/O	BLiTTER Configuration as follows: 

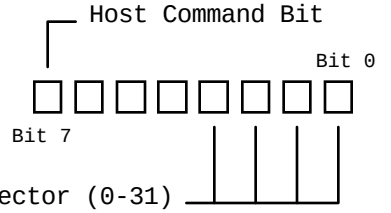
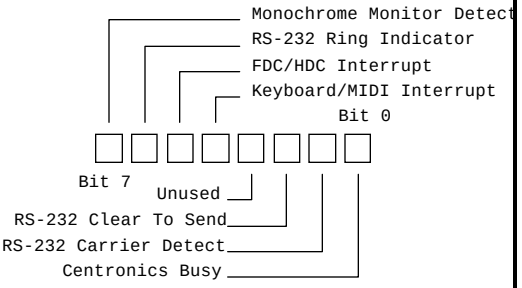
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF8A3D	**BYTE**							I/O	BLiTTER Configuration as follows: 
0x00FF8A3E– 0x00FF8BFF	**N/A**							I/O	Unassigned
SCC DMA Registers									
0x00FF8C00	**OB**							I/O	SCC DMA Pointer Upper
0x00FF8C02	**OB**							I/O	SCC DMA Pointer Upper-Middle
0x00FF8C04	**OB**							I/O	SCC DMA Pointer Lower-Middle
0x00FF8C06	**OB**							I/O	SCC DMA Pointer Lower
0x00FF8C08	**OB**							I/O	SCC Byte Count Upper
0x00FF8C0A	**OB**							I/O	SCC Byte Count Upper-Middle
0x00FF8C0C	**OB**							I/O	SCC Byte Count Lower-Middle
0x00FF8C0E	**OB**							I/O	SCC Byte Count Lower
0x00FF8C10	**WORD**							I/O	SCC Data Residue Register High (RO)
0x00FF8C12	**WORD**							I/O	SCC Data Residue Register Low (RO)
0x00FF8C14	**OB**							I/O	SCC DMA Control Register as follows: 
0x00FF8C16 – 0x00FF8C7E	**N/A**							I/O	Unassigned

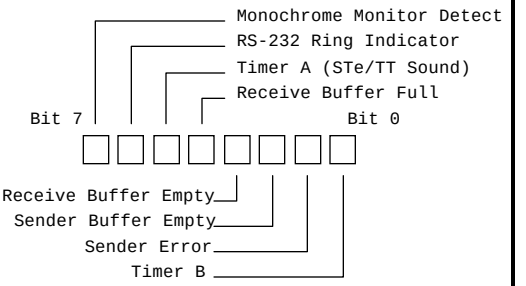
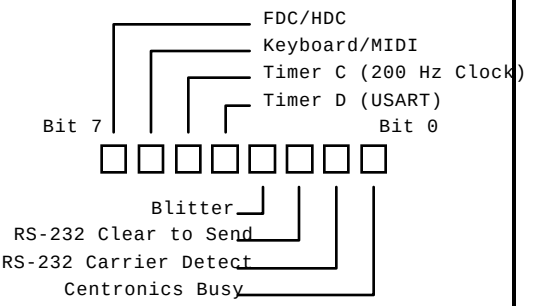
B.34 – Memory Map

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
SCC Ports (85C30)									
0x00FF8C80	**OB**							I/O	SCC A Control
0x00FF8C82	**OB**							I/O	SCC A Data
0x00FF8C84	**OB**							I/O	SCC B Control
0x00FF8C86	**OB**							I/O	SCC B Data
0x00FF8C88 – 0x00FF8DFF	**N/A**							I/O	Unassigned
System Control Unit									
0x00FF8E00	**OB**							I/O	SCU System Interrupt Mask
0x00FF8E02	**OB**							I/O	SCU System Interrupt State (RO)
0x00FF8E04	**OB**							I/O	SCU System Interrupter: Set Bit #0 to generate VME interrupt IRQ1.
0x00FF8E06	**OB**							I/O	VME Interrupter: Set Bit #0 to generate VME interrupt IRQ3.
0x00FF8E08	**OB**							I/O	SCU General Purpose Register 1
0x00FF8E0A	**OB**							I/O	SCU General Purpose Register 2
0x00FF8E0C	**OB**							I/O	VME Interrupt Mask
0x00FF8E0E	**OB**							I/O	VME Interrupt State (RO)
0x00FF8E10 – 0x00FF8E1F	**N/A**								Unassigned
Mega STe Cache/Processor Control									
0x00FF8E20	**OB**							I/O	Mega STe Cache/Processor Control Register as follows: **Value** — **Meaning** 0xFF — 16 MHz w/Cache 0xFE — 16 MHz 0xF4 — 8 MHz
0x00FF8E22 – 0x00FF8EFF	**N/A**								Unassigned
Extended Joystick/Paddle/Light Gun Ports									
0x00FF9200	**WORD**							I/O	Joystick Fire Button Matrix Register
0x00FF9202	**WORD**							I/O	Joystick Direction Matrix Register
0x00FF9204 – 0x00FF920F	**N/A**							I/O	Unassigned
0x00FF9210	**WORD**							I/O	Paddle 0 X Direction
0x00FF9212	**WORD**							I/O	Paddle 0 Y Direction
0x00FF9214	**WORD**							I/O	Paddle 1 X Direction
0x00FF9216	**WORD**							I/O	Paddle 1 Y Direction

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FF9218 – 0x00FF921F	**N/A**							I/O	Unassigned
0x00FF9220	**WORD**							I/O	Light Gun/Pen X Position
0x00FF9222	**WORD**							I/O	Light Gun/Pen Y Position
0x00FF9224 – 0x00FF97FF	**N/A**								Unassigned
Falcon030 VIDEL Palette Registers									
0x00FF9800 – 0x00FF9BFC	**LONG**							I/O	Falcon030 Palette Registers 0-255 as follows: `RRRRRR-- GGGGGG-- -------- BBBBBB--`
0x00FF9C00 – 0x00FFA1FF	**N/A**							I/O	Unassigned

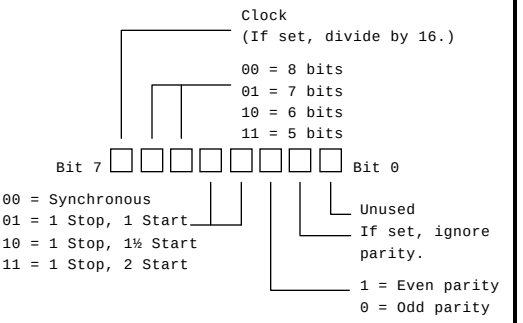
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
DSP Host Interface									
0x00FFA200	**BYTE**							I/O	Interrupt Control Register (DSP X:$FFE9) as follows: **Bit #7** INIT – Setting this bit forces initialization of the host interface. **Bits #6–5** DMA Mode Control as follows: **Value** **Meaning** %00 Interrupt Mode (DMA Off) %01 24-bit DMA Mode %10 16-bit DMA Mode %11 8-bit DMA Mode **Bit #4–3** Host Flags 1 & 0 respectively (HF1 & HF0) **Bit #2** Unused **Bits #1–0** Data Transfer Mode as follows: **Value** **Meaning in Interrupt Mode** %00 No Interrupts %01 Enable Receiver Full Interrupts %10 Enable Transmitter Empty Interrupts %11 Enable Both Interrupts **Value** **Meaning in DMA Mode** %00 No DMA %01 DSP to Host Request %10 Host to DSP Request

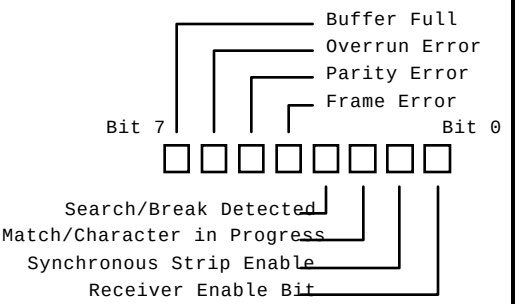
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFA201	**BYTE**							I/O	Command Vector Register (DSP X:$FFE9) as follows: 
0x00FFA202	**BYTE**							I/O	Interrupt Status Register (DSP X:$FFE8) as follows:
0x00FFA203	**BYTE**							I/O	Interrupt Vector Register (This register contains the 680x0 exception vector used for DSP exceptions).
0x00FFA204	**BYTE**							I/O	Unused
0x00FFA205	**BYTE**							I/O	DSP **WORD** High (DSP X:$FFEB)
0x00FFA206	**BYTE**							I/O	DSP **WORD** Middle (DSP X:$FFEB)
0x00FFA207	**BYTE**							I/O	DSP **WORD** Low (DSP X:$FFEB)
0x00FFA208 – 0x00FFF9FF	**N/A**							N/A	Undefined
ST Multi-Function Peripheral Port (68901)									
0x00FFFA00	**OB**							I/O	MFP-ST General Purpose Pins (Parallel port data register on Atari machines).
0x00FFFA02	**OB**							I/O	MFP-ST Active Edge Register as follows:  On a Falcon030, the MFP is not actually used for serial communcations.
0x00FFFA04	**OB**							I/O	MFP-ST Data Direction Register. Each bit is individually programmed (0 = input, 1 = output).

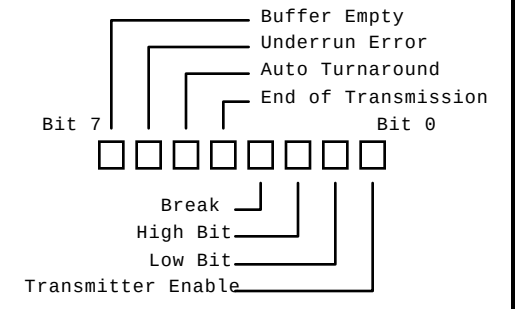
Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFA06	**OB**							I/O	MFP-ST Interrupt Enable Register A as follows:  On a Falcon030, the MFP is not actually used for serial communcations.
0x00FFFA08	**OB**							I/O	MFP-ST Interrupt Enable Register B as follows: 
0x00FFFA0A	**OB**							I/O	MFP-ST Interrupt Pending Register A (see mapping at 0x00FFFA06).
0x00FFFA0C	**OB**							I/O	MFP-ST Interrupt Pending Register B (see mapping at 0x00FFFA08).
0x00FFFA0E	**OB**							I/O	MFP-ST Interrupt In-Service Register A (see mapping at 0x00FFFA06).
0x00FFFA10	**OB**							I/O	MFP-ST Interrupt In-Service Register B (see mapping at 0x00FFFA08).
0x00FFFA12	**OB**							I/O	MFP-ST Interrupt Mask Register A (see mapping at 0x00FFFA06).
0x00FFFA14	**OB**							I/O	MFP-ST Interrupt Mask Register B (see mapping at 0x00FFFA08).

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFA16	**OB**							I/O	MFP-ST Vector Register. Bit 3 is set to 1 to indicate software End-of-Interrupt mode and 0 to indicate automatic End-of-Interrupt mode.
0x00FFFA18	**OB**							I/O	MFP-ST Timer A Control Register. Interpret bits 3-0 as follows: **Value Meaning** 0000 Timer stop. 0001 Delay mode, divide by 4. 0010 Delay mode, divide by 10. 0011 Delay mode, divide by 16. 0100 Delay mode, divide by 50. 0101 Delay mode, divide by 64. 0110 Delay mode, divide by 100. 0111 Delay mode, divide by 200. 1000 Event count mode. 1xxx Pulse extension mode (as above).
0x00FFFA1A	**OB**							I/O	MFP-ST Timer B Control Register (see Timer A).
0x00FFFA1C	**OB**							I/O	MFP-ST Timer C & D Control Register. Interpret bits 6-4 for Timer C and bits 2-0 for Timer D as follows: **Value Meaning** 000 Timer stop. 001 Delay mode, divide by 4. 010 Delay mode, divide by 10. 011 Delay mode, divide by 16. 100 Delay mode, divide by 50. 101 Delay mode, divide by 64. 110 Delay mode, divide by 100. 111 Delay mode, divide by 200.
0x00FFFA1E	**OB**							I/O	MFP-ST Timer A Data Register.
0x00FFFA20	**OB**							I/O	MFP-ST Timer B Data Register.
0x00FFFA22	**OB**							I/O	MFP-ST Timer C Data Register.
0x00FFFA24	**OB**							I/O	MFP-ST Timer D Data Register.
0x00FFFA26	**OB**							I/O	MFP-ST Sync Character Register.

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFA28	**OB**							I/O	MFP-ST USART Control Register as follows:
0x00FFFA2A	**OB**							I/O	MFP-ST Receiver Status Register as follows:
0x00FFFA2C	**OB**							I/O	MFP-ST Transmitter Status Register as follows:



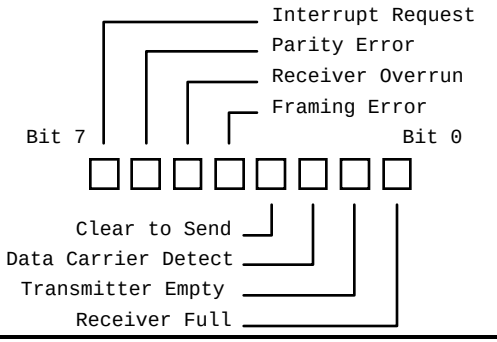


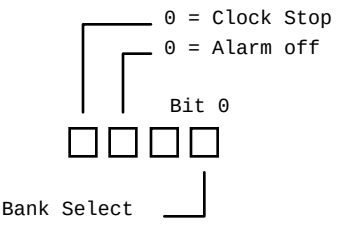


Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFA2E	**OB**							I/O	MFP-ST USART Data Register.
0x00FFFA30 – 0x00FFFA3F	**N/A**							I/O	Unassigned
68881 Math Co-Processor in Peripheral Mode									
0x00FFFA40	**WORD**							I/O	FPCIR Status Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA42	**WORD**							I/O	FPCTL Control Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA44	**WORD**							I/O	FPSAV Save Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA46	**WORD**							I/O	FPREST Restore Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA48	**WORD**							I/O	FPOPR Operation Word Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA4A	**WORD**							I/O	FPCMD Command Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA4C	**WORD**							I/O	FPRES Reserved (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA4E	**WORD**							I/O	FPCCR Condition Code Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA50	**LONG**							I/O	FPOP Operand Register (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA54	**WORD**							I/O	FPSLCT Register Select (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA56	**WORD**							I/O	Reserved
0x00FFFA58	**LONG**							I/O	FPIADR Instruction Address (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA5C	**LONG**							I/O	FPOADR Operand Address (available as a Mega Bus card accessed in 68881 peripheral mode)
0x00FFFA54 – 0x00FFFA7F	**N/A**							I/O	Unassigned
TT030 Multi-Function Peripheral Port (68901)									
0x00FFFA80	**OB**							I/O	MFP-TT030 GPIP (see 0x00FFFA00).
0x00FFFA82	**OB**							I/O	MFP-TT030 AER (see 0x00FFFA02).
0x00FFFA84	**OB**							I/O	MFP-TT030 DDR (see 0x00FFFA04).
0x00FFFA86	**OB**							I/O	MFP-TT030 IERA (see 0x00FFFA06).
0x00FFFA88	**OB**							I/O	MFP-TT030 IERB (see 0x00FFFA08).
0x00FFFA8A	**OB**							I/O	MFP-TT030 IPRA (see 0x00FFFA0A).
0x00FFFA8C	**OB**							I/O	MFP-TT030 IPRB (see 0x00FFFA0C).

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFA8E	**OB**							I/O	MFP-TT030 ISRA (see 0x00FFFA0E).
0x00FFFA90	**OB**							I/O	MFP-TT030 ISRB (see 0x00FFFA10).
0x00FFFA92	**OB**							I/O	MFP-TT030 IMRA (see 0x00FFFA12).
0x00FFFA94	**OB**							I/O	MFP-TT030 IMRB (see 0x00FFFA14).
0x00FFFA96	**OB**							I/O	MFP-TT030 VR (see 0x00FFFA16).
0x00FFFA98	**OB**							I/O	MFP-TT030 TACR (see 0x00FFFA18).
0x00FFFA9A	**OB**							I/O	MFP-TT030 TBCR (see 0x00FFFA1A).
0x00FFFA9C	**OB**							I/O	MFP-TT030 TCDCR (see 0x00FFFA1C).
0x00FFFA9E	**OB**							I/O	MFP-TT030 TADR (see 0x00FFFA1E).
0x00FFFAA0	**OB**							I/O	MFP-TT030 TBDR (see 0x00FFFA20).
0x00FFFAA2	**OB**							I/O	MFP-TT030 TCDR (see 0x00FFFA22).
0x00FFFAA4	**OB**							I/O	MFP-TT030 TDDR (see 0x00FFFA24).
0x00FFFAA6	**OB**							I/O	MFP-TT030 SCR (see 0x00FFFA26).
0x00FFFAA8	**OB**							I/O	MFP-TT030 UCR (see 0x00FFFA28).
0x00FFFAAA	**OB**							I/O	MFP-TT030 RSR (see 0x00FFFA2A).
0x00FFFAAC	**OB**							I/O	MFP-TT030 TSR (see 0x00FFFA2C).
0x00FFFAAE	**OB**							I/O	MFP-TT030 UDR (see 0x00FFFA2E).
0x00FFFAB0–0x00FFFBFF	**N/A**							I/O	Undefined

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
Keyboard ACIA (6850)									
0x00FFFC00	**EB**							I/O	Keyboard ACIA Control (when written) as follows: **Bit #7** Enables receive interrupts **Bits #6–5** Configures transmitter interrupts as follows: **Value** – **Meaning** %00 – RTS low, Disable Interrupts %01 – RTS low, Enable Interrupts %10 – RTS high, Disable Interrupts %11 – RTS low, Disable Interrupts Send a break on Interrupt **Bits #4–2** Configure Port Settings as follows: **Value** – **Data Bits–Parity–Stop Bits** %000 – 7-E-2 %001 – 7-O-2 %010 – 7-E-1 %011 – 7-O-1 %100 – 8-N-2 %101 – 8-N-1 %110 – 8-E-1 %111 – 8-O-1 **Bits #1–0** Set Clock Divisor as follows: **Value** – **Meaning** %00 – Normal %01 – Divide by 16 %10 – Divide by 256 %11 – Master Reset

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
									Keyboard ACIA Control (when read) as follows: 
0x00FFFC02	**EB**							I/O	Keyboard ACIA Data
MIDI ACIA (6850)									
0x00FFFC04	**EB**							I/O	MIDI ACIA Control (see keyboard ACIA control register for details)
0x00FFFC06	**EB**							I/O	MIDI ACIA Data
Mega ST Real Time Clock (RP5C15)									
0x00FFFC20	**OB**							I/O	Bank 0: Seconds-Ones (0–9) Bank 1: Clock output frequency as follows: **Value** — **Meaning** 0 — Open-Collector "CLKOUT" 1 — 16384 Hz 2 — 1024 Hz 3 — 128 Hz 4 — 16 Hz 5 — 1 Hz 6 — 1/60 Hz 7 — Open-Collector "CLKOUT"
0x00FFFC22	**OB**							I/O	Bank 0: Seconds-Tens (0–5) Bank 1: Setting bit #0 will reset the seconds register to the 0 and, if the seconds register is currently between 30–59, increment the minutes register.
0x00FFFC24	**OB**							I/O	Bank 0: Minutes-Ones (0–9) Bank 1: Alarm Minutes-Ones (0–9)

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFC26	**OB**							I/O	Bank 0: Minutes–Tens (0–5) Bank 1: Alarm Minutes-Tens (0–5)
0x00FFFC28	**OB**							I/O	Bank 0: Hour-Ones (0–9) Bank 1: Alarm Hour-Ones (0–9)
0x00FFFC2A	**OB**							I/O	Bank 0: Hour-Tens (0–2), in 24 hour mode, otherwise (0–1) in 12 hour mode with Bit 1 being set for PM, cleared for AM. Bank 1: Alarm Hour-Tens (as in bank 0)
0x00FFFC2C	**OB**							I/O	Bank 0: Day of Week (0–6), 0 = Sunday Bank 1: Alarm Day of Week (0–6), 0 = Sunday
0x00FFFC2E	**OB**							I/O	Bank 0: Date-Ones (0–9) Bank 1: Alarm Date-Ones (0–9)
0x00FFFC30	**OB**							I/O	Bank 0: Date-Tens (0–3) Bank 1: Alarm Date-Tens (0–3)
0x00FFFC32	**OB**							I/O	Bank 0: Month-Ones (0–9) Bank 1: Not Used
0x00FFFC34	**OB**							I/O	Bank 0: Month-Tens (0–1) Bank 1: If Bit #1 is set then clock is in 24 hour mode, otherwise, it is in 12 hour mode.
0x00FFFC36	**OB**							I/O	Bank 0: Year-Ones (0–9). The value for Year represents the (Year - 1980). Bank 1: Leap Year Register (0–3), 0 = Leap Year
0x00FFFC38	**OB**							I/O	Bank 0: Year-Tens (0–9) Bank 1: Not Used
0x00FFFC3A	**OB**							I/O	Mode Register as follows: 
0x00FFFC3C	**OB**							I/O	Test Register (lower nibble must equal zero to show confirm proper functioning)

Location(s)	Size	ST	Mega ST	STe	Mega STe	TT030	Falcon030	Type	Meaning
0x00FFFC3E	**OB**							I/O	Reset Register as follows: 0 = 1 Hz Alarm Pulse 0 = 16 Hz Alarm Pulse Bit 0 1 = Clock Reset 1 = Alarm Reset
0x00FFFC40– 0x00FFFFFF	**N/A**							I/O	Undefined
Expansion Area									
0x01000000 – 0x01FFFFFF	**N/A**							RAM	TT030 Fast Ram (Unsuitable for direct DMA and Video Shifter transfers)
0x02000000 – 0xFDFFFFFF	**N/A**							RSVD	Reserved
0xFE000000 – 0xFEFEFFFF	**N/A**							VME	VME A24:D16 Addressable Area
0xFEFF0000 – 0xFEFFFFFF	**N/A**							VME	VME A16:D16 Addressable Area
Shadow Image									
0xFF000000 – 0xFFFFFFFF	**N/A**							Image	This area is a 'shadow' image of 0x00000000 – 0x00FFFFFF to remain compatible with the ST.